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Performance analysis of a thermoelectric cooler with a corrugated architecture

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HIGHLIGHTS

• We model a unique hybrid thermoelectric architecture with a corrugated structure.

• COP of the corrugated TE similar to conventional "bulk" TE module.

• Cooling power density of corrugated TE shown to be much lower than a bulk TE.

• Heat transfer coefficient of the corrugated TE lower than bulk TE for typical applications.

• Corrugated TE shown to have potential fabrication and implementation benefits.

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ABSTRACT

A thermoelectric (TE) cooler architecture is presented that employs thin film thermoelectric elements on a plastic substrate in a corrugated structure sandwiched between planar thermal interface plates. This design represents a hybrid of a conventional bulk TE device and an in-plane thin film TE design. This design is attractive as it may benefit from low cost thin-film processing in a roll-to-roll fashion onto low-cost plastics substrates while maintaining a cross-plane heat flux for large area applications and a geometry that assists in maintaining a significant temperature difference across the thermoelectric elements. First, the performance of a single thermocouple is analyzed and the effect of the parasitic heat loss through the plastic substrate is examined. The performance of an array of thermocouples is then considered and the effects of various geometric parameters are analyzed with particular focus on the packing density of thermoelectric legs. The results show that while the coefficient of performance (COP) is comparable to a conventional bulk element TE cooler, the cooling power density drops off dramatically with a decrease in stacking angle of the legs. A comparison is then made between the heat sink demands of the hybrid TE design and a conventional bulk TE device where it is found that the lower cooling power density of the hybrid TE results in a reduction of heat sink demands as compared to bulk TE modules. The modeled performance suggest that the hybrid TE device may be advantageous in low cooling power density applications over relatively large areas where the low-cost nature of the device is maximized and less elaborate heat sink designs work effectively, cumulatively improving cost competitiveness.

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1. Introduction

Thermoelectric (TE) devices convert a heat flux into electric power or conversely convert electric power into a heat flux [1–3], with an illustration of a conventional TE module given in Fig. 1a. TEs possess a number of advantages over other energy conversion technologies such as the absence of moving parts, low maintenance, and the potential for precise temperature control [1,4,5]. However, a major hurdle for thermoelectric devices is the

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http://dx.doi.org/10.1016/j.apenergy.2015.01.132 0306-2619/© 2015 Elsevier Ltd. All rights reserved. low efficiency resulting in a large cost per unit of converted power [6,7]. This has lead to considerable research devoted to the development of high performance TE materials [8–11]. While advanced materials can lead to improved efficiency [8], they are often cost prohibitive. One promising materials focus is to employ efficient thin film TE elements that are compatible with scalable low-cost processing methods [12–17]. In addition, research beyond materials has included device geometry optimization, where structural optimization ranges from modification of the TE legs [18,19] to alternative module designs (e.g. non-planar geometries) [20–22]. An example of module design includes ring-structured TE elements







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Nomenclature		Creek symbols	
Sumbols		A	Seebeck coefficient
Δ Δ	cross-sectional area of thermoelement	δ	length of thermoelectric couple contact region
Δ	area of thermoelectric module	Δ	change in a property
Γ_m	coefficient of performance	$\overline{\theta}$	angle of inclination of the legs with the horizontal
D	overall length of hybrid thermoelectric module	λ	length of a hybrid thermocouple projected onto the
D H	height of thermoelectric module		horizontal plane.
I	current flowing through the thermocouple	0	electrical resistivity
I K	thermal conductance	σ	thermal conductivity
1	length of one thermoelement in the simplified architec-	τ	thickness of a thermoelement
·	ture	τ_{s}	thickness of thermoelement substrate
n	number of thermocouples	5	
P	input electrical power into thermocouple	Subscripts	
a.	cooling power of a single thermocouple	c cold side	
$\hat{0}_{\alpha}$	cooling power of an array of thermocouples	h	hot side
$\vec{0}'$	cooling power density for an array of thermocouples	max	maximum
\tilde{R}^{c}	electrical resistance	n	<i>n</i> -type semiconductor
Т	absolute temperature	n	<i>n</i> -type semiconductor
Ū,	cold-side overall heat transfer coefficient	r S	substrate
Ŵ	width of a thermoelement	∞	values of a property at ambient conditions
			······

that are optimized to harvest energy from circular cross sections such as oil pipelines and vehicle exhaust pipes [21,22].

In thin film TE designs, the thin film elements are typically deposited on a supporting substrate where the direction of heat transfer can be either in the plane of the film or across the plane



Fig. 1. Illustrations of (a) a conventional bulk thermoelectric (B-TE) cooling module, (b) an in-plane thin film thermoelectric (IP-TE) device removing heat from a heat source, and (c) the proposed corrugated thermoelectric (C-TE) cooling module.

of the film. Thin film in-plane TE coolers have been shown to be useful in cooling devices such as infrared detectors, solid-state lasers, low-noise amplifiers and micro-electromechanical systems where the heat dissipation is low and the devices performance is significantly enhanced with moderate temperature reductions [23–26]. However, the lateral position of the thermoelectric legs in in-plane TEs restricts the ability to populate many thermocouples over large areas. Thin film TEs can also be employed with cross-plane heat fluxes that are compatible with large area applications, but the thin film nature results in difficulty in maintaining a significant temperature difference across the legs [27], which can limit device performance as discussed below. Yet, the ability to place the thin films on various substrate materials and geometries opens up TE module design possibilities. For example, thin film thermoelectric materials have been deposited on a fiber substrate allowing for integration into textiles [28].

A promising low-cost thin-film thermoelectric architecture that has been demonstrated is based on TE elements printed on a corrugated substrate that is sandwiched between two thermal interface plates, illustrated in Fig. 1c [17,29-31]. This structure can be thought of as a combination of a conventional "bulk" thermoelectric (B-TE) device (Fig. 1a) and an in-plane thin-film thermoelectric (IP-TE) design (Fig. 1b) [23-26], where the thin film forms a corrugated geometry and thus labeled here as a corrugated thermoelectric (C-TE) device. The conventional B-TE modules are typically composed of pellet shaped thermoelectric legs sandwiched between two thermal interface plates where heat transfer is across the plane of the plates. This architecture is the most widely commercially available TE technology. In the C-TE design, heat transfer is in the plane of the thermoelectric supporting substrate similar to IP-TEs but with cross-plane heat transfer with a significant leglength similar to B-TEs. This design effectively removes the lateral leg constraint associated with the IP-TE design and provides a means to effectively maintain a substantial temperature difference across the thermoelectric leg.

In this paper, the performance of the C-TE structure is theoretically analyzed from a single thermoelectric couple to a thermoelectric module. There have been experimental demonstrations of



Fig. 2. Top, an illustration of the corrugated TE module with a sinusoidal leg geometry. Bottom, an illustration representing a trapezoidal wave approximation of the thermoelectric legs to analytically model device performance. The bottom figure includes characteristic dimensions used in the performance analysis.

similar architectures for power generation applications showing good agreement with theoretical predictions [17,31]. The previous results support the use of a theoretical analysis to explore geometric device optimization and extrapolation of the expected performance for various materials and geometries, which is considered here for the first time. The C-TE module investigated consists of *n*-type and *p*-type semiconductor legs printed on top of a wavestructured plastic substrate in an alternating fashion with metal interconnects resulting in thermoelectric legs with a pattern analogous to the conventional B-TE structure, as shown in Fig. 2. The structure is then sandwiched between thin plastic thermal interface plates. While TE devices can work for both power generation and cooling, a focus in this paper is on cooling. This is due in part to the expected performance as discussed below and temperature limitations of the device due to the implementation of plastic components. Both analytical and finite element computational models are developed and the geometric parameters of the C-TE design are varied. Results show that this architecture can have performance comparable to a conventional B-TE in applications that require low cooling power density. The analysis of heat transfer with the local environment also shows that for large-area applications elaborate heat exchanger designs may be avoided reducing system costs. In addition, the C-TE device is compatible with low cost fabrication methods, such as screen-printing and inkjet printing [13,32]. Combined, these results suggest the C-TE cooler may have a competitive advantage for large-area low heat flux density applications due to the potential of reduced device fabrication costs and reduced balance of system costs.

2. Device architecture and governing equations

2.1. Materials and architecture

It is expected that during implementation of the C-TE design, the wave-structured substrate will form a sinusoidal shape [17,29]. However, in order to analytically examine the effect of the geometric parameters, the architecture is simplified by approximating the shape as a trapezoidal wave structure with straight thermoelectric elements as illustrated in Fig. 2. In practice, a sinusoidal shape may be favored to avoid sharp curves that could be points of device failure during fabrication and operation. However, as described below, the straight-line approximation

Table 1

Properties of *n*-type and *p*-type thermoelements and the PET substrate.

<i>p-Type properties</i> Seebeck coefficient Electrical conductivity Thermal conductivity	220 $\mu V \ K^{-1}$ 8.826 Ωm 1.472 $W m^{-1} \ K^{-1}$
n-Type properties Seebeck coefficient Electrical conductivity Thermal conductivity	$\begin{array}{c} -223 \ \mu V \ K^{-1} \\ 8.239 \ \Omega m \\ 1.643 \ Wm^{-1} \ K^{-1} \end{array}$
Other property PET thermal conductivity	$0.2 \ Wm^{-1} \ K^{-1}$

results in a relatively small difference in predicted device performance. The major dimensions of the C-TE module are shown in Fig. 2 and include the total length (*D*), height (*H*), and width (*B*). Dimensions of a single thermocouple include the length of each thermoelement (*l*), the wavelength of the thermocouple (λ), the contact length of the thermoelectric elements with the thermal interface layer (δ), the angle between the legs and the thermal interface layer (θ), the semiconductor thickness (τ), and the substrate thickness (τ_s). The material properties for the C-TE module are given in Table 1. The *p*-type and *n*-type semiconductor properties chosen are similar to other reports [4,33], and result in a thermoelectric figure of merit (*Z*T) of approximately 1 at 300 K; values that are typical for currently available thermoelectric materials [4,6]. The plastic substrate and thermal interface layer are taken as polyester (PET).

2.2. Governing equations

Depending on the application, the performance metrics that are optimized for thermoelectric coolers include the cold side cooling power (Q_c), the coefficient of performance (*COP*), and the maximum temperature difference between the hot and cold sides [4,24,34,35]. The governing equations for thermoelectric energy conversion used to obtain these performance metrics have been extensively covered elsewhere [4,36], and we only present a brief review here. The cooling power of a single thermocouple is given by,

$$q_{c} = I\alpha T_{c} - K(T_{h} - T_{c}) - 0.5I^{2}R$$
(1)

where *I* is the current, α is the Seebeck coefficient, *T* is the absolute temperature, *K* is the combined thermal conductance of the legs and the substrate, and *R* is the electrical resistance. The subscripts *c* and *h* refer to the cold side and the hot side of the thermoelectric legs, respectively. For an array of thermocouples the cooling power density is given by,

$$Q_c' = nq_c/A_m \tag{2}$$

where *n* is the number of thermocouples and A_m is the area of the module. To find the *COP* of the device, we need to account for the input power (*P*) given by,

$$P = n[\alpha I(T_h - T_c) + I^2 R].$$
(3)

The *COP* is then equal to Q_c/P , where Q_c is the total cooling power. In Eq. (1), *K* and *R* are given by,

$$K = \rho_p \frac{\tau_p w_p}{l_p} + \rho_n \frac{\tau_n w_n}{l_n} + 2\rho_s \frac{\tau_s w_s}{l_s},\tag{4}$$

and

$$R = R_p + R_n = \sigma_p \frac{l_p}{\tau_p w_p} + \sigma_n \frac{l_n}{\tau_n w_n},$$
(5)

where ρ and σ are the thermal and electrical resistivity of the elements, and *w* is the width of the thermoelectric leg. The subscripts *n*

and *p* refer to the *n*-type and *p*-type semiconductors, and *s* refers to the substrate.

In our analysis of the C-TE cooler we make the following commonly applied assumptions: (1) constant material properties, (2) negligible contact resistances, (3) Thompson effects can be ignored, and (4) the effects of convection and radiation between thermoelements are not significant. While materials properties will change with temperature, assumption (1) and (3) is valid at the temperature range being considered here. Assumption (2) can be made because we are dealing with relatively long thermoelectric legs, and assumption (4) is reasonable if we also assume that the temperature differences involved are relatively low thereby reducing the effects of convection and radiation.

In the analysis of the proposed device, the straight leg approximation is compared to the sinusoidal structure, where the sinusoidal structure is analyzed computationally with a finite element model (FEM) with the geometry created in SolidWorks[®] (SolidWorks Co., X64, 2013) and energy conversion analysis completed using the built in thermoelectric solver in ANSYS[®] (ANSYS Inc., V14.5, 2014). Additional details of the FEM are provided below.

3. Results and discussion

3.1. Single thermocouple characteristics

We begin the analysis of the C-TE architecture by considering a single thermocouple. The initial focus on one couple will assist in gaining insight into loss mechanisms associated with the thermoelement substrate and differences between the computational and analytical analysis. The legs are modeled with a length of $l_p = l_n = 5$ mm, a width w = 15 mm, and a thickness of $\tau = 75 \,\mu$ m. In general thicker semiconductor films and shorter leg lengths will result in larger cooling power, as discussed below. Consequently, the selected dimensions are chosen to ensure significant cooling power density while being representative of an achievable C-TE device [29], as well as having a leg length similar to conventional B-TE modules [6,27]. The thermoelectric legs are considered for 2 cases: (1) films deposited on a 75 μ m thick PET substrate, and (2) free standing thermoelectric films. The boundary conditions are taken as constant temperature on the hot and cold side surfaces. In the analytical analysis, the thermoelement stacking angle (θ) is not required to describe the system as heat transfer along the couple is solely conduction and can be described by Eq. (1). The cooling power (q_c) and COP are given as a function of current through the device in Fig. 3, for the case of a hot side temperature T_h = 300 K and a range of cold side temperatures. Results are given using the analytical approximation and using FEM. The FEM is based on the geometry pictured in Fig. 4 (with $\theta \approx 75^{\circ}$) and is comprised of 140,188 nodes and 25,160 elements. Further refinement of the mesh to 353,840 nodes and 70,560 elements resulted in a change in q_c of less than 0.5% suggesting a converged solution. It is found that the difference between the analytical and numerical results is generally less than 1% showing negligible difference associated with the straight-leg approximation. In Fig. 3 it is apparent that performance is hindered by parasitic heat transfer through the substrate, where the maximum performance in terms of q_c and *COP* both occur with $T_c = T_h = 300$ K (i.e. no parasitic losses through the substrate). For a cold junction temperature of 273 K (0 °C), the maximum COP of the hybrid thermocouple is 1.06. For a representative bulk device with identical leg length and material properties, but with a thermoelement cross-sectional area (A_c) of 3 mm by 3 mm [27], the maximum COP of the thermocouple is 1.19. Thus, the maximum COP of the C-TE couple is approximately 89% of a representative B-TE couple. The primary difference in performance



Fig. 3. (a) The cooling power of a single thermocouple (q_c) with variation in applied current. (b) The coefficient of performance (COP) of a single thermocouple vs. applied current. In both (a) and (b) the performance is given for a hot side temperature (T_h) of 300 K, and various cold side temperatures (T_c) . The performance is also given for the thermocouple with and without a substrate. Finally, the cooling power in (a) as predicted by finite element modeling (FEM) is also provided.

is due to the parasitic heat loss through the substrate, which as we move toward $T_c = T_h$, the difference in performance between the C-TE structure and the B-TE structure is reduced. For example, if the cold junction temperature is increased to 285 K, the maximum *COP* of the C-TE couple is 2.8, which represents 93% of the B-TE couple.

A closer look at the finite element model provides additional insight into the thermoelectric couple behavior. First, the deviation between the analytical model and the finite element model is primarily due to the assumption in Eq. (2), that half of the joule heat generated in a thermocouple flows to the cold side while the remaining half goes to the hot side. Since the cold junction temperature is lower than the hot junction temperature, the heat flux will be slightly greater toward the cold junction resulting in a slightly reduced prediction of the cooling power. The temperature profile along the length of the thermoelectric legs as obtained from FEM is given in Fig. 4 for T_c = 273 K and highlights this non-symmetric temperature profile. Also observed in Fig. 4 is that the maximum temperature in the *p*-type semiconductor is higher than that in the *n*-type semiconductor, which is expected due to the higher electrical resistance of the *p*-type material. Finally, the maximum cooling power that the thermocouple can achieve $(q_{c,max})$ for various



Fig. 4. Temperature profile along the length of the thermoelectric leg from cold side to hot side for the boundary conditions of T_c = 273 K and T_h = 300 K. Inset, temperature profile for the thermoelectric couple as predicted by finite element modeling.



Fig. 5. The maximum cooling power of a single couple $(q_{c,max})$ vs. the temperature difference across the thermocouple (ΔT) is given for different thermoelectric leg thicknesses. The solid lines represent a substrate-supported device while the dashed lines represent a free-standing device. The vertical gap between a set of same-colored dashed and solid lines represent heat transfer losses due to thermal conduction through the substrate. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

temperature differences and thermoelectric legs is given in Fig. 5. As with a bulk device, the maximum heat removal decreases with increasing temperature difference, as expected. Also as expected, a reduction in cooling power due to parasitic heat transfer through the substrate is more pronounced when the ratio of thermoelectric element thickness to substrate thickness decreases. However, these results show that even with a temperature difference across the device of 50 K, the percentage of cooling power loss associated with the substrate can be smaller than 10% if the ratio of the thermoelectric element to substrate thickness is greater than 1:1.

3.2. C-TE module performance characteristics

At its core the difference between the B-TE cooling module and C-TE cooling module is the geometry of the active layers. Under the limiting case of the C-TE module with a thermoelement angle

 θ = 90°, no substrate present, and a net spacing between the thin film elements equivalent to a comparable B-TE module, the theoretical performance of the C-TE and B-TE devices are the same. This geometric dependence can be appreciated by considering Eq. (2) and the maximum cooling power ($Q_{c,max}$) of the device. In general the optimized current (I_{opt}) that produces $Q_{c,max}$ for a TE device is given by Lee [37],

$$I_{opt} = \frac{\alpha T_c}{R} \tag{6}$$

Since $R \propto A_c^{-1}$ and $K \propto A_c$, where A_c is the thermoelectric element cross-sectional area, it can be shown that holding other device properties constant results in $Q_{c,max} = n[aA_c - bA_c - cA_c]$, where the coefficients a, b and c are constant. Here, it is clearly seen that the maximum heat transfer possible for a TE module is linearly proportional to the net cross section area of the thermoelectric elements. Thus the cooling power of the C-TE module is directly related to how closely the thermoelectric layers can be stacked.

In terms of the C-TE architecture, the packing density will depend primarily on θ , with secondary dependence on δ , τ , and $\tau_{\rm s}$. The effect of these geometric parameters on the maximum cooling power of the TE module is given in Fig. 6 for a module with a leg length of l = 5 mm and under the boundary conditions of T_h = 300 K and T_c = 273 K (i.e. from room temperature to freezing water). In Fig. 6a, the cooling power density as a function of θ is given for various semiconductor thicknesses (τ), no thermoelectric substrate, and δ set to be the combined thickness of the *p*-type and *n*-type thermoelectric elements. The performance of a B-TE module is also provided in Fig. 6a for a module with the same semiconductor properties, leg length l = 5 mm, and A_c of 3 mm by 3 mm. The spacing between the bulk elements is varied from an ideal case of no spacing between elements to a spacing of 1 mm. In Fig. 6b, the dependence of the maximum cooling power density on θ is given for a similar geometry as that in Fig. 6a, but with the inclusion of the thermoelectric substrate, τ_s = 75 μ m, and a variation in δ . Finally, in Fig. 6c the maximum cooling density is given with δ = 1.5 mm and a variation in τ , and τ_{s} .

From Fig. 6, it is clear that a high stacking angle of the C-TE legs is critical for high cooling power density. As shown in Fig. 6a, the performance of the B-TE array for thermocouples with no spacing coincides with the C-TE device when θ = 90°, which is tantamount to the theoretical no-space condition. As the TE leg stacking-angle of the C-TE reduces, there is a sharp drop in the maximum heat flux density of the device. Even as the B-TE leg spacing increases to 1 mm, the angle of the legs (θ) for the C-TE module must remains very close to 90° to meet the heat flux density of the B-TE device. For example, a C-TE module with an angle θ = 75° and τ = 75 μ m, the maximum heat flux is approximately 10 times lower than the B-TE module with an element spacing of 1 mm. Fig. 6 also highlights the sensitivity of the contact length of the legs (δ) to the overall cooling power density of the module. This impact of δ becomes more significant at high leg angles due to the fact that δ becomes the dominant geometric feature dictating the thermoelectric leg packing density. This would suggest that minimizing δ would maximize performance. However, decreasing the contact region may significant reduce the ability to effectively transfer heat to and away from the thermoelectric elements and thus reduce performance. As shown in the finite element model in Fig. 4, the temperature profile of the thermal interface plane when using a PET thermal interface film clearly shows a cold spot at the thermoelectric leg contact region. This is due to the thermal resistance of the plastic interface plates that limits efficient lateral heat transfer. The performance analysis given in Fig. 6 assumes heat is efficiently spread to and away from the thermoelectric legs. As discussed below, the thin plastic film has a relatively low cross-plane thermal resistance due



Fig. 6. The maximum cooling power density $(Q_{c,max})$ of the hybrid-thermoelectric (C-TE) module as a function of the angle of inclination of the legs. The performance in (a) is for the ideal scenario of $\delta = 2\tau$. The horizontal lines in (a) is the performance of a comparable bulk TE module with thermoelement cross-sectional area of 3.0 mm by 3.0 mm, and thermoelement leg spacing of 0 mm (solid line), 0.5 mm (dashed line) and 1 mm (dotted line). (b) Cooling power density with $\tau = 75$ mm, $\tau_s = 0$ mm and a variation in the thermoelectric couple contact width, δ . (c) The cooling power density with $\delta = 1.5$ mm and a variation in thermoelement thickness (τ_s).

to its small thickness, however heat removal once heat is transferred across this plate is critical to optimize module performance. Lateral heat spreading will be improved with the addition of exterior metal films or other heat sink design on the plastic interface plates [7]. In general, heat spreading in thermoelectrics has been found to be an important source of performance loss when the TE-module fill factor (the summed cross-sectional area of the thermoelements to the total device cross-sectional area) is below approximately 1% [7]. This is under the assumption that a high thermal conductivity thermal interface layer is employed. Here, the fill factor (*F*) of the C-TE module can be defined as $F \approx \tau / [\delta - \tau + l\cos(\theta)]$. Under this definition, *F* drops very quickly with θ . For example, *F* falls below 10% for the case of $\delta = 2\tau$ when $\theta < 82^{\circ}$. However, *F* stays above 1% for broad range of geometric designs. Thus, lateral heat spreading is not expected to be a source of significant performance loss over the range of C-TE geometries that are likely to be employed, as long as the thermal conductivity of the thermal interface layer is made sufficiently high [6,7].

As shown in Fig. 3, reducing the current below the maximum cooling power density in general results in an increase in COP. Thus, when the C-TE and B-TE modules have a similar cooling power density, the COP of the B-TE module may be greater than the C-TE module due to the ability to operate well below its maximum cooling power density. However, the B-TE module will have substantially more semiconductor per unit volume resulting in the device being more expensive. Reducing the TE-module fill factor has been previously been shown to be a highly effective way of reducing device costs [7]. However, a full cost optimization is required to interrogate this trade-off and will be a focus of future work. Summarizing the thermoelectric cooling module performance, the C-TE can be designed to have a COP comparable to the B-TE but with relatively low cooling power density for realistic device architectures ($\theta < 80^\circ$, $\delta > 0.25$ mm). While the cooling power density may be significantly reduced, this is compatible with the key advantage of the C-TE design of low-cost processing of large area devices.

3.3. Heat sink consideration

In any thermoelectric application, a key factor of the system performance is the ability to minimize thermal resistance between the thermoelectric module and its environment [1]. This is typically accomplished by forced convection over the module and maximizing the thermal interface exposed surface area (i.e. heat fins and other heat exchanger design) [33,38]. However, in many cases TE modules operate in a heat sink limited regime, i.e. employed where the thermal heat sink between the TE module and the local environment restricts heat transfer across the thermoelectric device, and results in a reduction in the maximum cooling power density (or power generation) [27].

In the C-TE design, the low cooling power density associated with the device architecture should relieve the heat exchanger design requirements with the local environment. To consider the effect of cooling power density on heat transfer to the environment, the thermal resistance between the cold side of the TE device and the environment can be effectively represented by the cold side overall heat transfer coefficient (U_c), where $Q_c = U_c A_m (T_c - T_{c,\infty})$, and $T_{c,\infty}$ is the cold side ambient temperature. Here, we compare the effect of U_c on the device performance for the C-TE and B-TE cooling modules. The C-TE module is modeled with τ = 75 μ m, l = 5 mm, w = 15 mm, a spacing between rows of thermoelectric legs of 1 mm, δ = 1.5 mm, θ = 75°, and *n* = 532. This results in a maximum cooling power of $Q_{c,max}$ = 41 W when the boundary conditions are constant surface temperature of T_h = 300 K, and T_c = 273 K. This is compared to a B-TE module with the same leg length of l = 5 mm, $A_c = 3 \text{ mm}$ by 3 mm, and a spacing between elements of 0.75 mm. To obtain an equivalent maximum cooling power as the C-TE module, n = 67. This results in a C-TE cooling module area of approximately 400 cm², and a B-TE module area of approximately 19 cm². Note this results in a similar net

thermoelectric material volume between the C-TE and B-TE modules. The constant surface temperature boundary conditions used above eliminate the need to consider heat exchange with the local environment. To introduce the thermal resistance between the thermoelectric and the environment we focus on the cold side of the device. The hot side is assumed to have an effective heat sink and the constant surface temperature boundary condition remains. On the cold side, $T_{c,\infty}$ is set to 273 K, and the surface temperature will be dependent on U_c . If Q_c is eliminated in Eq. (2) by substituting $Q_c = U_c A_m (T_c - T_{c,\infty})$, T_c can be shown to depend on U_c by,

$$T_{c} = \frac{U_{c}A_{m}T_{\infty,c} + n(0.5l^{2}R + KT_{h})}{n(l\alpha + K) + U_{c}A_{m}}$$
(7)

Values of T_c for various values of U_c are then obtained and used to determine the cooling power. The result of this analysis is given in Fig. 7 showing that the U_c required for the TE module to transfer a significant amount of heat is much lower for the C-TE module than the comparable B-TE module. To achieve a cooling rate, which is 75% of the ideal case of negligible heat sink thermal resistance, the U_c for the C-TE and B-TE are 78 Wm⁻² K⁻¹ and 1680 $\text{Wm}^{-2} \text{K}^{-1}$ respectively. This difference in U_c is proportional to the difference in module area of the devices. In Fig. 7, the vertical dashed and dotted lines represent approximate U_c values for natural convection for air and water. The natural convection estimations were arrived at by assuming an isothermal surface and that the device is placed such that the cold side thermal interface layer is vertical [39]. It is important to note that B-TE modules usually use ceramic thermal interface plates while the C-TE module employs PET interface layers, as discussed above. These materials will have approximate thermal conductivities of 100 Wm⁻¹ K⁻¹ and 0.2 $Wm^{-1} K^{-1}$, respectively [39]. For a thickness of 500 μm for the plastic plate and 1 mm for the ceramic plate [40], the thermal resistance across the plates are $2.75 \times 10^{-3} \text{ m}^2 \text{ K W}^{-1}$ and $1 \times 10^{-4} \,\text{m}^2 \,\text{KW}^{-1}$ for the C-TE and B-TE module, respectively. Thus, for the sake of comparison and because they are comparatively low when considering the overall thermal resistance, they are ignored in this analysis. In addition, it is assumed the outer surface temperature is constant along the interface layer. While lateral heat spreading will be an important factor to mitigate when using plastic thermal interface layers, this feature is not considered in this analysis. The values of U_c for air-cooled and water-cooled



Fig. 7. Cooling power of an C-TE module and a B-TE module with change in the cold side overall heat transfer coefficient (U_c) for the boundary conditions of $T_{c,\infty}$ = 293 K, and T_h = 300 K. Representative U_c values for natural convection of air and water on a vertical surface of the C-TE module is also provided as reference.

conditions for the C-TE module are found to be $5.4 \text{ W m}^{-2} \text{ K}^{-1}$ and 175 W $m^{-2} K^{-1}$, resulting in the cold-side junction temperature of 232 K and 268 K and heat transfer being 21% and 83% of the limiting no thermal resistance scenario, respectively. Performing a similar analysis for the B-TE module assuming a square module, U_c for air-cooled and water-cooled conditions is found to be $5.8 \text{ W} \text{ m}^{-2}\text{K}^{-1}$ and $427 \text{ W} \text{ m}^{-2}\text{K}^{-1}$ respectively. This resulted in a cold junction temperature of 220 K and 247 K with the cooling being 1.5% and 49% of the ideal case, respectively. These results show that an elaborate heat exchange system may not be needed for the cold side in low cooling power applications. For cooling applications the hot side will have a greater heat flux demand, and greater heat transfer coefficients will be required for effective performance. This is due to the higher Peltier heat flux and the additional joule heating dissipation. However, a similar trend between heat transfer coefficients observed on the cold side between the C-TE and B-TE will exist on the hot side of the device.

It is important to note that the dimensions of the B-TE module can be varied to change the fill factor of the device such that, assuming efficient heat spreading, designs are possible that will remove the need for elaborate heat exchanger designs. However, the C-TE approach has the potential to allow for simple and effective means of changing the packing density for a given application by altering the thermoelement leg stacking angle.

3.4. Design advantages of the C-TE module

There are several key design advantages of the C-TE module beyond the energy conversion performance. These advantageous include the compatibility with low-cost processing, simple modification of the packing density of the TE elements, and the ability to form mechanically resilient modules that can take non-planar shapes [30]. As mentioned above, low-cost thin film printing methods such as inkjet printing, screen-printing, and doctor blading [12,13,15,32,41] can be used to deposit the active layers while in a planar form. These methods are compatible with roll-to-roll processing, which is widely recognized as a low-cost large area manufacturing approach [42]. The planar elements can then be formed into a sinusoidal shape and adhered to the thermal interface layers. This approach is effective as long as the elements are flexible. Bending the elements after printing has previously been demonstrated for organic [15], inorganic [13,14], and hybrid organic-inorganic [43] thermoelectric elements. In many cases, the power density of a given application is unique and optimal performance can be found for a specific packing density of TE elements. Employing the C-TE architecture where θ can be varied prior to final implementation allows for a simple means to effectively control F, to meet application specific requirements. An added benefit of the C-TE design and materials employed is the increased mechanical resilience as compared to conventional B-TE modules. A B-TE module is typically comprised of crystalline semiconductor legs and ceramic thermal interface plates that are brittle. In contrast, the thin film elements and plastic components of the C-TE allow for improved flexibility, where a previous demonstration of a C-TE module with 38 thermocouples with a patterned thermal interface layer design was shown to maintain electrical properties when flexed to a 9 mm radius of curvature [29]. For an application that requires flexibility, the use of a heat sinks are likely prohibitive, in which case the lower packing density of the C-TE elements that removes the need for elaborate heat sinks would be appropriate.

4. Conclusion

In this paper we investigated the performance of a novel hybrid thermoelectric cooler, which involves the use of semiconductor

films printed on plastic substrates with a sinusoidal geometry. The performance of the device is compared to a conventional bulk thermoelectric device. We show that parasitic heat transfer through the substrate in the C-TE module is a source of performance losses, but can be minimized with proper thickness selection. The heat flux capabilities of the device are also shown to be highly sensitive to the angle of the thermoelectric legs (θ) and the contact area of the legs to the thermal interface plates (δ). For practical device geometries, the C-TE module cooling power density is substantially lower than a B-TE module, but with this lower flux comes reduced heat transfer requirements between the device and the environment. This result leads to the large area modules being effective without requiring advanced heat sink designs. These results suggest that the C-TE module may be advantageous in applications where a low cooling power density is required over a relatively large area. This large area application space of the C-TE design approach compliments the compatibility of this device architecture with scalable roll-to-roll thin-film processing methods [12,14,44], and flexible device applications where heat sinks may be incompatible.

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